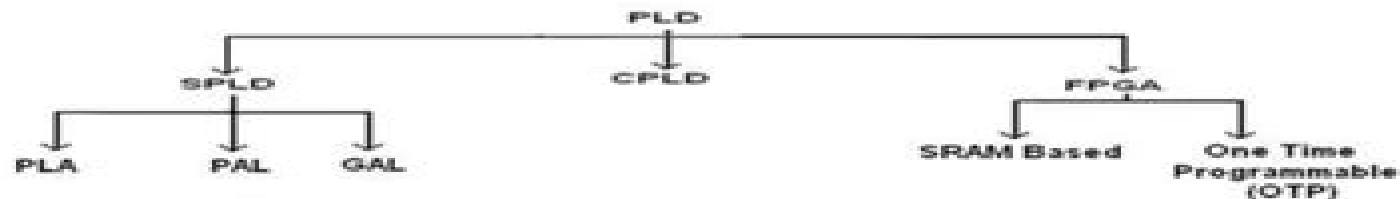Dr. Y.Narasimha Murthy Ph.D
yayavaram@yahoo.com

UNIT-1 CPLD & FPGA ARCHITECTURE & APPLICATIONS

Introduction : The need of programmable devices was realized in early 70s itself with the design of PLD by **Ron Cline from Signetics** . The digital ICs like TTL or CMOS have fixed functionality and the user has no option to change or modify their functionality .i.e they work according to the design given by the manufacturer. So,to change this people started thinking of a methodology by which the functionality of an IC can be modified or changed. Then the concept of using Fuses in ICs entered and gained momentum. This method of changing or modifying the functionality of an IC using the Fuses was appreciated and this method of blowing a Fuse between two contacts or keeping the Fuse intact was done by using a software and hence these devices were called Programmable Logic Devices(PLDs).

Many digital chips were considered under the category of PLDs .But the most fundamental and primitive was the Memories like ROM or PROM etc.

The realization of Digital circuits by PLDs can be classified as shown in the diagram below.

PLAs were introduced in the early 1970s, by Philips, but their main drawbacks were that they were expensive to manufacture and offered somewhat poor speed-performance. Both disadvantages were due to the two levels of configurable logic, because programmable logic planes were difficult to manufacture and introduced significant propagation delays. To overcome these problems , Programmable Array Logic (PAL) devices were developed.

Memory : Memory is used to store, provide access to, and allow modification of data and program code for use within a processor-based electronic circuit or system. The two basic types of memory are ROM (read–only memory) and RAM (random access memory).

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Clive Maxfield

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   FPGA ... ,2006   *Proceedings* ,1999   **Electrical & Electronics Abstracts** ,1997   *Designing with FPGAs and CPLDs* Jesse H. Jenkins,1994 This text covers the entire field of FPGAs and is intended to bring designers and engineers up to speed in this area It describes all products within a comparative framework that highlights the strengths and weaknesses of individual FPGAs and their application potential   **FPGAs: World Class Designs** Clive Maxfield,2009-02-24 All the design and development inspiration and direction a harware engineer needs in one blockbuster book Clive Max Maxfield renowned author columnist and editor of PL DesignLine has selected the very best FPGA design material from the Newnes portfolio and has compiled it into this volume The result is a book covering the gamut of FPGA design from design fundamentals to optimized layout techniques with a strong pragmatic emphasis In addition to specific design techniques and practices this book also discusses various approaches to solving FPGA design problems and how to successfully apply theory to actual design tasks The material has been selected for its timelessness as well as for its relevance to contemporary FPGA design issues ContentsChapter 1 Alternative FPGA ArchitecturesChapter 2 Design Techniques Rules and GuidelinesChapter 3 A VHDL Primer The EssentialsChapter 4 Modeling MemoriesChapter 5 Introduction to Synchronous State Machine Design and AnalysisChapter 6 Embedded ProcessorsChapter 7 Digital Signal ProcessingChapter 8 Basics of Embedded Audio ProcessingChapter 9 Basics of Embedded Video and Image ProcessingChapter 10 Programming Streaming FPGA Applications Using Block Diagrams In SimulinkChapter 11 Ladder and functional block programmingChapter 12 Timers Hand picked content selected by Clive Max Maxfield character luminary columnist and author Proven best design practices for FPGA development verification and low power Case histories and design examples get you off and running on your current project   Designing with FPGAs and CPLDs Bob Zeidman,2002-01-09 Choose the right programmable logic devices and development tools Understand the design verification and testing issues Plan schedules and allocate resources efficiently Choose the right programmable logic devices with this guide to the technolog   FPGAs and Parallel Architectures for Aerospace Applications Fernanda Kastensmidt,Paolo Rech,2015-12-07 This book introduces the concepts of soft errors in FPGAs as well as the motivation for using commercial off the shelf COTS FPGAs in mission critical and remote applications such as aerospace The authors describe the effects of radiation in FPGAs present a large set of soft error mitigation techniques that can be applied in these circuits as well as methods for qualifying these circuits under radiation Coverage includes radiation effects in FPGAs fault tolerant techniques for FPGAs use of COTS FPGAs in aerospace applications experimental data of FPGAs under radiation FPGA embedded processors under radiation and fault injection in FPGAs Since dedicated parallel processing architectures such as GPUs have become more desirable in aerospace applications due to high computational power GPU analysis under radiation is also discussed   *Tree-based Heterogeneous FPGA Architectures* Umer Farooq,Zied Marrakchi,Habib Mehrez,2012-05-14 This book presents a new FPGA architecture known as tree based

FPGA architecture due to its hierarchical nature This type of architecture has been relatively unexplored despite their better performance and predictable routing behavior as compared to mesh based FPGA architectures In this book we explore and optimize the tree based architecture and we evaluate it by comparing it to equivalent mesh based FPGA architectures

FPGA Architecture Ian Kuon,2008   Application-Specific Mesh-based Heterogeneous FPGA Architectures Husain Parvez,Habib Mehrez,2010-11-05 This book presents a new exploration environment for mesh based heterogeneous FPGA architectures It describes state of the art techniques for reducing area requirements in FPGA architectures which also increase performance and enable reduction in power required Coverage focuses on reduction of FPGA area by introducing heterogeneous hard blocks such as multipliers adders etc in FPGAs and by designing application specific FPGAs Automatic FPGA layout generation techniques are employed to decrease non recurring engineering NRE costs and time to market of application specific heterogeneous FPGA architectures   FPGA Design Automation Deming Chen,Jason Cong,Peichen Pan,2006 FPGA Design Automation A Survey is an up to date comprehensive survey tutorial of FPGA design automation with an emphasis on the recent developments within the past 5 to 10 years The focus is on the theory and techniques that have been or most likely will be reduced to practice It covers all major steps in FPGA design flow routing and placement circuit clustering technology mapping and architecture specific optimization physical synthesis RT level and behavior level synthesis and power optimization FPGA Design Automation A Survey can be used as both a guide for beginners who are embarking on research in this relatively young yet exciting area and a useful reference for established researchers in this field   *Partial Reconfiguration on FPGAs* Dirk Koch,2012-07-25 This is the first book to focus on designing run time reconfigurable systems on FPGAs in order to gain resource and power efficiency as well as to improve speed Case studies in partial reconfiguration guide readers through the FPGA jungle straight toward a working system The discussion of partial reconfiguration is comprehensive and practical with models introduced together with methods to implement efficiently the corresponding systems Coverage includes concepts for partial module integration and corresponding communication architectures floorplanning of the on FPGA resources physical implementation aspects starting from constraining primitive placement and routing all the way down to the bitstream required to configure the FPGA and verification of reconfigurable systems

3D-CAD U. Sendler,1993-10-01   *Field-Programmable Gate Arrays* John V. Oldfield,Richard C. Dorf,1995-01-23 Due to unique advantages like security improved testing and reprogrammability field programmable gate arrays are making broad inroads in the electronics industry This comprehensive overview of the topic explains the underlying principles strengths and limitations of a range of FPGA architectures Includes abundant references and illustrations   **A Tiled Fpga Architecture for Power-aware Computations** ,2006 Current SRAM FPGAs have reached high gate densities which make them suitable for portable reconfigurable systems and data intensive applications However some challenges need to be faced to make this become a reality First due to a large number of transistors for field programmability and low utilization rate of FPGA

resources existing FPGAs are highly power hungry compared to ASICs As chip technology progresses to 90 nm and below this situation becomes worse and static current plays a major role in the total power Second the present column based configuration structure is not flexible enough for applications with multiple reconfigurations Unnecessary memory bits have to be configured if the layout of the module does not fully occupy the height of the device and consequently introduces wastage of time and energy Third the global clock distribution over the whole chip results in a very high power consumption Even when some parts of the hardware resources are not used the whole clock line must be switched at every clock cycle Finally current FPGAs can not support bus routing structure The implementation of data intensive applications using traditional bit based routing tracks will require more routing resource and produce higher power consumption A lot of previous efforts have been made on FPGA power modeling and power reduction In the work of power modeling and estimation for SRAM FPGAs none of them has considered the impact of inrush current and configuration current which can not be neglected for low power applications that need multiple reconfigurations For the previous power reduction architectures some of them considered either one of dynamic power reduction or static power reduction The other architectures such as dual Vdd FPGA architecture considered both dynamic power and static power reduction But their implementations produce significant area and configuration time overheads and the power management strategy is very inefficient since it is based on fine grained logic blocks or routing switches The complex power management makes these architectures not practical for the real time applications that need multiple dynamic reconfigurations This thesis proposes a battery aware tiled FPGA architecture for data intensive computations The architecture is globally coarse grained in terms of FPGA tiles and locally fine grained in terms of configurable logic blocks within each FPGA tile The main feature of the architecture is that the power supply to each tile can be turned on off depending on the computational requirements and system load The static control strategy is fairly simple which makes the area and configuration time overheads relatively small The architecture adopts a two level configuration structure column based programming and fully random access programming which can efficiently reduce the configuration time and energy while keeping the overheads of pin count and area relatively small This combined configuration architecture enables the easy task relocation from one tile to another The top level routing architecture between tiles is a combined bus based and bit based routing structure which is very efficient for data intensive applications A simulation platform is built with NetLogo to evaluate the proposed architecture Besides dynamic and static currents inrush and configuration currents are also considered The static control function is implemented in the platform to reflect the main feature of the architecture which is the coarse grained power supply control strategy Experimental results on some randomly generated task graphs and a JPEG encoder show that 1 tradeoff between execution time and power battery usage can be achieved by using different number of tiles in the architecture 2 significant savings in battery energy cost can be achieved by using the static control function provided by the architecture 3 by varying the

architectural parameters of the tiled FPGA more savings in battery energy cost could be obtained *Principles and Structures of FPGAs* Hideharu Amano,2018 This comprehensive textbook on the field programmable gate array FPGA covers its history fundamental knowledge architectures device technologies computer aided design technologies design tools examples of application and future trends Programmable logic devices represented by FPGAs have been rapidly developed in recent years and have become key electronic devices used in most IT products This book provides both complete introductions suitable for students and beginners and high level techniques useful for engineers and researchers in this field Differently developed from usual integrated circuits the FPGA has unique structures design methodologies and application techniques Allowing programming by users the device can dramatically reduce the rising cost of development in advanced semiconductor chips The FPGA is now driving the most advanced semiconductor processes and is an all in one platform combining memory CPUs and various peripheral interfaces This book introduces the FPGA from various aspects for readers of different levels Novice learners can acquire a fundamental knowledge of the FPGA including its history from Chapter 1 the first half of Chapter 2 and Chapter 4 Professionals who are already familiar with the device will gain a deeper understanding of the structures and design methodologies from Chapters 3 and 5 Chapters 6 8 also provide advanced techniques and cutting edge applications and trends useful for professionals Although the first parts are mainly suitable for students the advanced sections of the book will be valuable for professionals in acquiring an in depth understanding of the FPGA to maximize the performance of the device FPGAs Juan Jose Rodriguez Andina,Eduardo de la Torre Arnanz,Maria Dolores Valdes,2016-05-15 This book explains the how and why of field programmable gate array FPGA usage It analyzes fundamental architectures of FPGA devices providing case studies and simple design examples It also describes advanced features of the latest devices exploring new resources enabling problem solving in new application domains such as high speed sensor interfacing and control of power converters From basic circuits to state of the art implementations this text demystifies FPGAs for engineers who are not digital designers but need efficient digital solutions for their systems to be competitive *A Fault Tolerant FPGA Architecture* Md. Tanveer Anwar,2008 Architecture and CAD for Deep-Submicron FPGAS Vaughn Betz,Jonathan Rose,Alexander Marquardt,1999-03-31 Architecture and CAD for Deep Submicron FPGAs addresses several key issues in the design of high performance FPGA architectures and CAD tools with particular emphasis on issues that are important for FPGAs implemented in deep submicron processes Three factors combine to determine the performance of an FPGA the quality of the CAD tools used to map circuits into the FPGA the quality of the FPGA architecture and the electrical i e transistor level design of the FPGA Architecture and CAD for Deep Submicron FPGAs examines all three of these issues in concert **Optimizing FPGA Architecture for Deep Learning Workloads** Aman Arora,2023 Deep Learning DL applications have tremendous computation requirements making running them on traditional computers CPUs very inefficient Modern computer systems deploy hardware acceleration which involves offloading compute intensive and

memory intensive tasks to specialized hardware In the space of hardware acceleration alternatives Field Programmable Gate Arrays FPGAs lie in the middle of the programmability efficiency spectrum with Graphic Processing Units GPUs being more programmable and Application Specific Integrated Circuits ASICs being more efficient FPGAs provide massive parallelism and are reconfigurable which makes them very well suited for the fast changing needs of DL applications However the generic building blocks available on traditional FPGAs limit the acceleration that can be achieved Hence FPGAs trail ASICs by an order of magnitude in terms of performance So how can the gap between ASICs and FPGAs be minimized while retaining the strength of FPGAs the reconfigurability This dissertation describes research that aims to find the answer to this question by proposing new domain optimized FPGAs for Deep Learning The key idea is to integrate new hardware blocks to the FPGA that provide domain specialized functionality while still keeping them largely general and allowing them to be used with traditional FPGA flows Specifically new DL optimized FPGAs containing blocks called Tensor Slices and CoMeFa RAMs are presented The architecture of these blocks along with the tradeoffs in exploring their architectures is explained Results show that significant performance improvement and energy reduction can be obtained for DL applications by using DL specialized FPGAs containing these blocks New benchmarks called Koios developed to explore FPGA architectures for DL are also explained These benchmarks are open sourced and work with VTR an academic open source FPGA architecture exploration tool New DL optimized FPGAs containing Tensor Slices and CoMeFa RAMs are significantly more efficient at accelerating DL workloads while still being reconfigurable at a fine grain With the abundance of DL applications making DL optimized FPGAs is an attractive proposition

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