Finite State Machine Datapath Design, Optimization, and Implementation

Justin Davis
Robert B. Reese

Finite State Machine Datapath Design Optimization And Implementation Synthesis Lectures On Digital Circuits And Systems

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   Finite State Machine Datapath Design, Optimization, and Implementation Justin Davis,Robert Reese,2007-06-01 Finite State Machine Datapath Design Optimization and Implementation explores the design space of combined FSM Datapath implementations The lecture starts by examining performance issues in digital systems such as clock skew and its effect on setup and hold time constraints and the use of pipelining for increasing system clock frequency This is followed by definitions for latency and throughput with associated resource tradeoffs explored in detail through the use of dataflow graphs and scheduling tables applied to examples taken from digital signal processing applications Also design issues relating to functionality interfacing and performance for different types of memories commonly found in ASICs and FPGAs such as FIFOs single ports and dual ports are examined Selected design examples are presented in implementation neutral Verilog code and block diagrams with associated design files available as downloads for both Altera Quartus and Xilinx Virtex FPGA platforms A working knowledge of Verilog logic synthesis and basic digital design techniques is required This lecture is suitable as a companion to the synthesis lecture titled Introduction to Logic Synthesis using Verilog HDL Table of Contents Calculating Maximum Clock Frequency Improving Design Performance Finite State Machine with Datapath FSMD Design Embedded Memory Usage in Finite State Machine with Datapath FSMD Designs   **Finite State Machine Datapath Design, Optimization, and Implementation** Justin Davis,Robert Reese,2022-05-31 Finite State Machine Datapath Design Optimization and Implementation explores the design space of combined FSM Datapath implementations The lecture starts by examining performance issues in digital systems such as clock skew and its effect on setup and hold time constraints and the use of pipelining for increasing system clock frequency This is followed by definitions for latency and throughput with associated resource tradeoffs explored in detail through the use of dataflow graphs and scheduling tables applied to examples taken from digital signal processing applications Also design issues relating to functionality interfacing and performance for different types of memories commonly found in ASICs and FPGAs such as FIFOs single ports and dual ports are examined Selected design examples are presented in implementation neutral Verilog code and block diagrams with associated design files available as downloads for both Altera Quartus and Xilinx Virtex FPGA platforms A working knowledge of Verilog logic synthesis and basic digital design techniques is required This lecture is suitable as a companion to the synthesis lecture titled Introduction to Logic Synthesis using Verilog HDL Table of Contents Calculating Maximum Clock Frequency Improving Design Performance Finite State Machine with Datapath FSMD Design Embedded Memory Usage in Finite State Machine with Datapath FSMD Designs   **Embedded Systems Interfacing for Engineers using the Freescale HCS08 Microcontroller I** Douglas Summerville,2022-06-01 This textbook provides practicing scientists and engineers an advanced treatment of the Atmel AVR microcontroller This book is intended as a follow on to a previously

published book titled Atmel AVR Microcontroller Primer Programming and Interfacing Some of the content from this earlier text is retained for completeness This book will emphasize advanced programming and interfacing skills We focus on system level design consisting of several interacting microcontroller subsystems The first chapter discusses the system design process Our approach is to provide the skills to quickly get up to speed to operate the internationally popular Atmel AVR microcontroller line by developing systems level design skills We use the Atmel ATmega164 as a representative sample of the AVR line The knowledge you gain on this microcontroller can be easily translated to every other microcontroller in the AVR line In succeeding chapters we cover the main subsystems aboard the microcontroller providing a short theory section followed by a description of the related microcontroller subsystem with accompanying software for the subsystem We then provide advanced examples exercising some of the features discussed In all examples we use the C programming language The code provided can be readily adapted to the wide variety of compilers available for the Atmel AVR microcontroller line We also include a chapter describing how to interface the microcontroller to a wide variety of input and output devices The book concludes with several detailed system level design examples employing the Atmel AVR microcontroller Table of Contents Embedded Systems Design Atmel AVR Architecture Overview Serial Communication Subsystem Analog to Digital Conversion ADC Interrupt Subsystem Timing Subsystem Atmel AVR Operating Parameters and Interfacing System Level Design **Designing Asynchronous Circuits using NULL Convention Logic (NCL)** Scott Smith,Jia Di,2022-06-01 Designing Asynchronous Circuits using NULL Convention Logic NCL begins with an introduction to asynchronous clockless logic in general and then focuses on delay insensitive asynchronous logic design using the NCL paradigm The book details design of input complete and observable dual rail and quad rail combinational circuits and then discusses implementation of sequential circuits which require datapath feedback Next throughput optimization techniques are presented including pipelining embedding registration early completion and NULL cycle reduction Subsequently low power design techniques such as wavefront steering and Multi Threshold CMOS MTCMOS for NCL are discussed The book culminates with a comprehensive design example of an optimized Greatest Common Divisor circuit Readers should have prior knowledge of basic logic design concepts such as Boolean algebra and Karnaugh maps After studying this book readers should have a good understanding of the differences between asynchronous and synchronous circuits and should be able to design arbitrary NCL circuits optimized for area throughput and power Table of Contents Introduction to Asynchronous Logic Overview of NULL Convention Logic NCL Combinational NCL Circuit Design Sequential NCL Circuit Design NCL Throughput Optimization Low Power NCL Design Comprehensive NCL Design Example *Developing Embedded Software using DaVinci and OMAP Technology* B.I. Pawate,2022-05-31 This book discusses how to develop embedded products using DaVinci OMAP Technology from Texas Instruments Incorporated It presents a single software platform for diverse hardware platforms DaVinci OMAP Technology refers to the family of processors development tools software products and support While DaVinci Technology is

driven by the needs of consumer video products such as IP network cameras networked projectors digital signage and portable media players OMAP Technology is driven by the needs of wireless products such as smart phones Texas Instruments offers a wide variety of processing devices to meet our users price and performance needs These vary from single digital signal processing devices to complex system on chip SoC devices with multiple processors and peripherals As a software developer you question Do I need to become an expert in signal processing and learn the details of these complex devices before I can use them in my application As a senior executive you wonder How can I reduce my engineering development cost How can I move from one processor to another from Texas Instruments without incurring a significant development cost This book addresses these questions with sample code and gives an insight into the software architecture and associated component software products that make up this software platform As an example we show how we develop an IP network camera Using this software platform you can choose to focus on the application and quickly create a product without having to learn the details of the underlying hardware or signal processing algorithms Alternatively you can choose to differentiate at both the application as well as the signal processing layer by developing and adding your algorithms using the xDAIS for Digital Media xDM guidelines for component software Finally you may use one code base across different hardware platforms Table of Contents Software Platform More about xDM VISA CE Building a Product Based on DaVinci Technology Reducing Development Cost eXpressDSP Digital Media xDM Sample Application Using xDM Embedded Peripheral Software Interface EPSI Sample Application Using EPSI Sample Application Using EPSI and xDM IP Network Camera on DM355 Using TI Software Adding your secret sauce to the Signal Processing Layer SPL Further Reading

Digital Circuits and Systems Mitchell Thornton,Justin Davis,Robert B. Reese,2010 This is the first volume in a new hardcover combined volume of Synthesis Lectures This volume contains the following lectures Finite State Machine Datapath Design Optimization and Implementation Introduction to Logic Synthesis using Verilog HDL High Speed Digital System Design Microcontrollers Fundamentals for Engineers and Scientists Proceedings of the ... Midwest Symposium on Circuits and Systems ,1996 **Logic Synthesis for FSM-Based Control Units** Alexander Barkalov,Larysa Titarenko,2009-11-25 This book presents the hardware implementation of control algorithms represented by graph schemes of algorithm It includes new methods of logic synthesis and optimization for logic circuits of Mealy and Moore FSMs oriented on both ASIC and FPLD Finite State Machine Logic Synthesis for Complex Programmable Logic Devices Robert Czerwinski,Dariusz Kania,2013-01-12 This book is a monograph devoted to logic synthesis and optimization for CPLDs CPLDs macrocell can also be interpreted as programmable AND fixed OR structure well known as PAL based structure The question is what should be done when the number of implicants representing function exceeds the number of product terms available in a logic block The answer is in the book Logic synthesis and optimization methods dedicated for PAL based structures are proposed The methods strive to find the optimum fit for the combinational logic and finite state machines to the structure of

the logic device and aim at area and speed optimization The theoretical background and complete strategies are richly illustrated with examples and figures **Logic Synthesis for VLSI-Based Combined Finite State Machines** Alexander Barkalov,Larysa Titarenko,Kamil Mielcarek,Małgorzata Mazurkiewicz,Elżbieta Kawecka,2022-11-24 The book is devoted to design and optimization of control units represented by combined finite state machines CFSMs The CFSMs combine features of both Mealy and Moore FSMs Having states of Moore FSM they produce output signals of both Mealy and Moore types To optimize the circuits of CFSMs we propose to use optimization methods targeting both Mealy and Moore FSMs The book contains some original synthesis and optimization methods targeting hardware reduction in VLSI based CFSM circuits These methods take into account the peculiarities of both a CFSM model and a VLSI chip in use The optimization is achieved due to combining classical optimization methods with new methods proposed in this book These new methods are a mixed encoding of collections of microoperations and a twofold state assignment in CFSMs All proposed methods target reducing the numbers of arguments in systems of Boolean functions representing CFSM circuits Also we propose to use classes of pseudoequivalent states of Moore FSMs to reduce the number of product terms in these systems The book includes a lot of examples which contributes to a better understanding of the features of the synthesis methods under consideration This is the first book entirely devoted to the problems associated with synthesis and optimization of VLSI based CFSMs We hope that the book will be interesting and useful for students and PhD students in the area of Computer Science as well as for designers of various digital systems We think that proposed CFSM models enlarge the class of models applied for implementation of control units with modern VLSI chips **Finite State Machines in Hardware** Volnei A. Pedroni,2013-12-20 A comprehensive guide to the theory and design of hardware implemented finite state machines with design examples developed in both VHDL and SystemVerilog languages Modern complex digital systems invariably include hardware implemented finite state machines The correct design of such parts is crucial for attaining proper system performance This book offers detailed comprehensive coverage of the theory and design for any category of hardware implemented finite state machines It describes crucial design problems that lead to incorrect or far from optimal implementation and provides examples of finite state machines developed in both VHDL and SystemVerilog the successor of Verilog hardware description languages Important features include extensive review of design practices for sequential digital circuits a new division of all state machines into three hardware based categories encompassing all possible situations with numerous practical examples provided in all three categories the presentation of complete designs with detailed VHDL and SystemVerilog codes comments and simulation results all tested in FPGA devices and exercise examples all of which can be synthesized simulated and physically implemented in FPGA boards Additional material is available on the book s Website Designing a state machine in hardware is more complex than designing it in software Although interest in hardware for finite state machines has grown dramatically in recent years there is no comprehensive treatment of the subject This book offers

the most detailed coverage of finite state machines available It will be essential for industrial designers of digital systems and for students of electrical engineering and computer science **Digital System Design using FSMs** Peter D. Minns,2021-06-23 DIGITAL SYSTEM DESIGN USING FSMS Explore this concise guide perfect for digital designers and students of electronic engineering who work in or study embedded systems Digital System Design using FSMs A Practical Learning Approach delivers a thorough update on the author s earlier work FSM Based Digital Design using Verilog HDL The new book retains the foundational content from the first book while including refreshed content to cover the design of Finite State Machines delivered in a linear programmed learning format The author describes a different form of State Machines based on Toggle Flip Flops and Data Flip Flops The book includes many figures of which 15 are Verilog HDL simulations that readers can use to test out the design methods described in the book as well as 19 Logisim simulation files with figures Additional circuits are also contained within the Wiley web folder It has tutorials and exercises including comprehensive coverage of real world examples demonstrated alongside the frame by frame presentations of the techniques used In addition to covering the necessary Boolean algebra in sufficient detail for the reader to implement the FSM based systems used in the book readers will also benefit from the inclusion of A thorough introduction to finite state machines and state diagrams for the design of electronic circuits and systems An exploration of using state diagrams to control external hardware subsystems Discussions of synthesizing hardware from a state diagram synchronous and asynchronous finite state machine designs and testing finite state machines using a test bench module A treatment of the One Hot Technique in finite state machine design An examination of Verilog HDL including its elements An analysis of Petri Nets including both sequential and parallel system design Suitable for design engineers and senior technicians seeking to enhance their skills in developing digital systems Digital System Design using FSMs A Practical Learning Approach will also earn a place in the libraries of undergraduate and graduate electrical and electronic engineering students and researchers Logic Synthesis for Finite State Machines Based on Linear Chains of States Alexander Barkalov,Larysa Titarenko,Jacek Bieganowski,2017-06-24 This book discusses Moore finite state machines FSMs implemented with field programmable gate arrays FPGAs including look up table LUT elements and embedded memory blocks EMBs To minimize the number of LUTs in FSM logic circuits the authors propose replacing a state register with a state counter They also put forward an approach allowing linear chains of states to be created which simplifies the system of input memory functions and therefore decreases the number of LUTs in the resulting FSM circuit The authors combine this approach with using EMBs to implement the system of output functions microoperations This allows a significant decrease in the number of LUTs as well as eliminating a lot of interconnections in the FSM logic circuit As a rule it also reduces the area occupied by the circuit and diminishes the resulting power dissipation This book is an interesting and valuable resource for students and postgraduates in the area of computer science as well as for designers of digital systems that included complex control units Sequential Logic Synthesis Pranav Ashar,S. Devadas,A. Richard

Newton,1992 Computer aided design CAD of very large scale integrated VLSI circuits is concerned with the development of computer programs for the automated design and manufacture of ICs Automated VLSI design is referred to as VLSI synthesis Synthesis of VLSI circuits involves transforming a specification of circuit behavior into a mask level layout which can be fabricated using VLSI manufacturing processes Optimization strategies are vital in VLSI synthesis in order to meet desired specifications However the optimization problems encountered in VLSI synthesis are typically nondeterministic polynomial time NP complete or NP hard Therefore solutions to the optimization problems incorporate heuristic strategies the development of which requires a thorough understanding of the problem at hand Thus optimization based VLSI synthesis has evolved into a rich and exciting area of research Automata theory forms a cornerstone of digital VLSI system design Sequential Logic Synthesis deals exclusively with finite automata theory and practice The extensive use of finite state automata finite state machines FSMs or simple sequential logic   Digital Electronics 3 Tertulien Ndjountche,2016-10-20 This third volume in the comprehensive Digital Electronics series which explores the basic principles and concepts of digital circuits focuses on finite state machines These machines are characterized by a behavior that is determined by a limited and defined number of states the holding conditions for each state and the branching conditions from one state to another They only allow one transition at a time and can be divided into two components a combinational logic circuit and a sequential logic circuit The approach is gradual and relatively independent of each other chapters To facilitate the assimilation and practical implementation of various concepts the book is complemented by a selection of practical exercises

Introduction to Noise-Resilient Computing Svetlana N. Yanushkevich,Seiya Kasai,Golam Tangim,A. H. Tran,2013 Noise abatement is the key problem of small scaled circuit design New computational paradigms are needed as these circuits shrink they become very vulnerable to noise and soft errors In this lecture we present a probabilistic computation framework for improving the resiliency of logic gates and circuits under random conditions induced by voltage or current fluctuation Among many probabilistic techniques for modeling such devices only a few models satisfy the requirements of efficient hardware implementation specifically Boltzman machines and Markov Random Field MRF models These models have similar built in noise immunity characteristics based on feedback mechanisms In probabilistic models the values 0 and 1 of logic functions are replaced by degrees of beliefs that these values occur An appropriate metric for degree of belief is probability We discuss various approaches for noise resilient logic gate design and propose a novel design taxonomy based on implementation of the MRF model by a new type of binary decision diagram BDD called a cyclic BDD In this approach logic gates and circuits are designed using 2 to 1 bi directional switches Such circuits are often modeled using Shannon expansions with the corresponding graph based implementation BDDs Simulation experiments are reported to show the noise immunity of the proposed structures Audiences who may benefit from this lecture include graduate students taking classes on advanced computing device design and academic and industrial researchers Table of Contents Introduction to

probabilistic computation models Nanoscale circuits and fluctuation problems Estimators and Metrics MRF Models of Logic Gates Neuromorphic models Noise tolerance via error correcting Conclusion and future work   High-Speed Digital System Design Justin Davis,2022-05-31 High Speed Digital System Design bridges the gap from theory to implementation in the real world Systems with clock speeds in low megahertz range qualify for high speed Proper design results in quality digital transmissions and lowers the chance for errors This book is for computer and electrical engineers who may or may not have learned electromagnetic theory The presentation style allows readers to quickly begin designing their own high speed systems and diagnosing existing designs for errors After studying this book readers will be able to Design the power distribution system for a printed circuit board to minimize noise Plan the layers of a PCB for signals power and ground to maximize signal quality and minimize noise Include test structures in the printed circuit board to easily diagnose manufacturing mistakes Choose the best PCB design parameters such a trace width height and routed path to ensure the most stable characteristic impedance Determine the correct termination to minimize reflections Predict the delay caused by a given PCB trace Minimize driver power consumption using AC terminations Compensate for discontinuities along a PCB trace Use pre emphasis and equalization techniques to counteract lossy transmission lines Determine the amount of crosstalk between two traces Diagnose existing PCBs to determine the sources of errors   **Digital Systems Design and Prototyping** Zoran Salcic,Asim Smailagic,2007-05-08 Digital Systems Design and Prototyping Using Field Programmable Logic and Hardware Description Languages Second Edition covers the subject of digital systems design using two important technologies Field Programmable Logic Devices FPLDs and Hardware Description Languages HDLs These two technologies are combined to aid in the design prototyping and implementation of a whole range of digital systems from very simple ones replacing traditional glue logic to very complex ones customized as the applications require Three HDLs are presented VHDL and Verilog the widely used standard languages and the proprietary Altera HDL AHDL The chapters on these languages serve as tutorials and comparisons are made that show the strengths and weaknesses of each language A large number of examples are used in the description of each language providing insight for the design and implementation of FPLDs With the addition of the Altera UP 1 prototyping board all examples can be tested and verified in a real FPLD Digital Systems Design and Prototyping Using Field Programmable Logic and Hardware Description Languages Second Edition is designed as an advanced level textbook as well as a reference for the professional engineer   *From Algorithm to Digital System* Samary Baranov,2020-11-24 This book is about how to use the Synthagate tool for the design of complex digital systems at the High Level and Register Transfer Level Specifically it demonstrates how to use Synthagate through the design of a processor to showcase the potential of Synthagate The main difference between Synthagate and other design tools is that the designer is not required to use hardware description languages Instead Synthagate uses Algorithmic State Machines ASMs at the different steps of design Synthagate covers most digital system designs from DSP to Processing Units This tool can be

used in the design of robots controllers processors IoT AI systems video and voice processing systems digital systems for automated and autonomous cars et cetera Most importantly not only experienced hardware designers but application engineers can design complex digital systems with Synthagate Synthagate can also be useful for students and educators of universities and colleges in courses such as Digital system design Systems on the chips VLSI system design Embedded systems Computer system architecture and many others How should you begin to work with the Synthagate tool and this book First you can download the Synthagate tool for two months for free at www synthezza com download synthagate If you are familiar with FSM and ASM head straight to Chapter 2 In the second chapter I demonstrate the design of a Processor with Synthagate in detail You can take the example of the same Processor in folder Cpu_4_16_8Altera in GUI ZIP from the benchmark s list www synthezza com hsl and rtl benchmarks and follow the step by step design guide explained in the second chapter Of course you can take any example from benchmarks and do the same Or try to design a device that has behavior you are familiar with If you have any ideas suggestions or comments we would be delighted to hear from you at support synthezza com   **Digital Systems** Jean-Pierre Deschamps,Elena Valderrama,Lluís Terés,2016-10-12 This textbook for a one semester course in Digital Systems Design describes the basic methods used to develop traditional Digital Systems based on the use of logic gates and flip flops as well as more advanced techniques that enable the design of very large circuits based on Hardware Description Languages and Synthesis tools It was originally designed to accompany a MOOC Massive Open Online Course created at the Autonomous University of Barcelona UAB currently available on the Coursera platform Readers will learn what a digital system is and how it can be developed preparing them for steps toward other technical disciplines such as Computer Architecture Robotics Bionics Avionics and others In particular students will learn to design digital systems of medium complexity describe digital systems using high level hardware description languages and understand the operation of computers at their most basic level All concepts introduced are reinforced by plentiful illustrations examples exercises and applications For example as an applied example of the design techniques presented the authors demonstrate the synthesis of a simple processor leaving the student in a position to enter the world of Computer Architecture and Embedded Systems

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