3.14 a. See Figure S.22.

Iteration	Instruction	Issues at	Executes/ Memory	Write CDB at	Comment
1	L.D F2.0(R1)	3.0	2	3	First issue
1	MUL.D F4,F2,F0	2	4	19	Wait for F2 Mult rs [3-4] Mult use [5-18]
18	L.D F6.0(R2)	3	4	5	Ldbuf [4]
1	ADD.D F6,F4,F6	4	20	30	Wait for F4 Add rs [5-20] Add use [21-29]
1	S.D F6,0(R2)	5	31		Wait for F6 Stbuf1 [6-31]
1	DADDIU R1,R1,#8	6	7	8	
1	DADDIU R2,R2,#8	7	. 8	9	
1	DSLTU R3,R1,R4	s	9	10	
1	BNEZ R3, foo	9	11		Wait for R3
2	L.D F2.0(R1)	10	12	13	Wait for BNEZ Ldbuf [11-12]
2	MUL.D F4,F2,F0	-11	44 19	34	Wait for F2 Mult busy Mult rs [12-19] Mult use [20-33]
2	L.D F6.0(R2)	12	13	1.4	Ldbuf [13]
2	ADD.D F6,F4,F6	13	35	45	Wait for F4 Add rs [14–35] Add use [36–44]
2	S.D F6,0(R2)	14	46		Wait for F6 Stbuf [15-46]
2	DADDIU R1,R1,#8	1.5	16	17	
2	DADDIU R2,R2,#8	16	17	18	
2	DSLTU R3,R1,R4	17	18	20	
2	BNEZ R3.foo	18	20		Wait for R3
3	L.D F2,0(R1)	19	21	22	Wait for BNEZ Ldbuf [20-21]
3	MUL.D F4,F2,F0	20	23 34	49	Wait for F2 Mult busy Mult rs [21-34] Mult use [35-48]
3	L.D F6.0(R2)	2.1	2.2	2.3	Ldbuf [22]
3	ADD.D F6,F4,F6	22	50	60	Wait for F4 Add rs [23-49] Add use [51-59]

Figure 5.22 Solution for exercise 3.14a.

Computer Architecture A Quantitative Approach Solution

J Elliott

Computer Architecture A Quantitative Approach Solution:

<u>Solutions to Selected Exercises in Computer Architecture</u> Thomas E. Willis, Allan D. Knies, 1996 This solution manual for the second edition of Computer Architecture A Quantitative Approach provides example solutions for many of the problems in the text The manual covers all eight chapters of CA AQA in addition to the two appendices that include exercises

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making decisions about the most appropriate jurisdictions in which to file patent applications. This book will also be of great value to computer professionals who are affected by the protection of software or who are actively involved in the protection Parallel Programming Thomas Rauber, Gudula R Nger, 2010-03-10 Innovations in hardware of software by patent law architecture like hyper threading or multicore processors mean that parallel computing resources are available for inexpensive desktop computers In only a few years many standard software products will be based on concepts of parallel programming implemented on such hardware and the range of applications will be much broader than that of scientific computing up to now the main application area for parallel computing Rauber and R nger take up these recent developments in processor architecture by giving detailed descriptions of parallel programming techniques that are necessary for developing efficient programs for multicore processors as well as for parallel cluster systems and supercomputers Their book is structured in three main parts covering all areas of parallel computing the architecture of parallel systems parallel programming models and environments and the implementation of efficient application algorithms. The emphasis lies on parallel programming techniques needed for different architectures The main goal of the book is to present parallel programming techniques that can be used in many situations for many application areas and which enable the reader to develop correct and efficient parallel programs Many examples and exercises are provided to show how to apply the techniques The book can be used as both a textbook for students and a reference book for professionals The presented material has been used for courses in parallel programming at different universities for many years **Process Algebra** ITI 2000 Damir Kalpić, Vesna Hljuz Dobrić, 2000 and Probabilistic Methods ,2002 **Operating Systems** Robert Switzer,1993 A theoretical and practical introduction to modern operating systems The system TUNIX provides the reader with a real operating system with which to experiment and includes demand paging and genuine multitasking Threads are implemented and used to achieve concurrency in a transparent fashion High-performance Computer Architecture Harold S. Stone, 1993 This update of the popular book on computer architecture presents design ideas embodied in many high performance machines and stresses techniques for evaluating them Stone develops a proper understanding of the design process by treating the various trade offs that exist in designing choices and shows how good designs make efficient use of technology Features Teaches techniques for the design and analysis of high performance machines Develops students intuition for design by treating various tradeoffs that exist in design choices Discusses many important topics RISC architectures interconnection meshes Cache coherent and multiprocessors and Cache Memory Includes enhanced descriptions of RISC Processors Expands material on Cache Memory Analysis Current technology in RISC with a focused look on super scalar Additional memory models and techniques for doing Cache design New porposals for coherent memory systems in System C parallel processors Both design and thought problems and problems with limiting parameters are Solving Linear Systems on Vector and Shared Memory Computers J. J. provided 0201526883B04062001

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