

Benefits of Key Value SSD

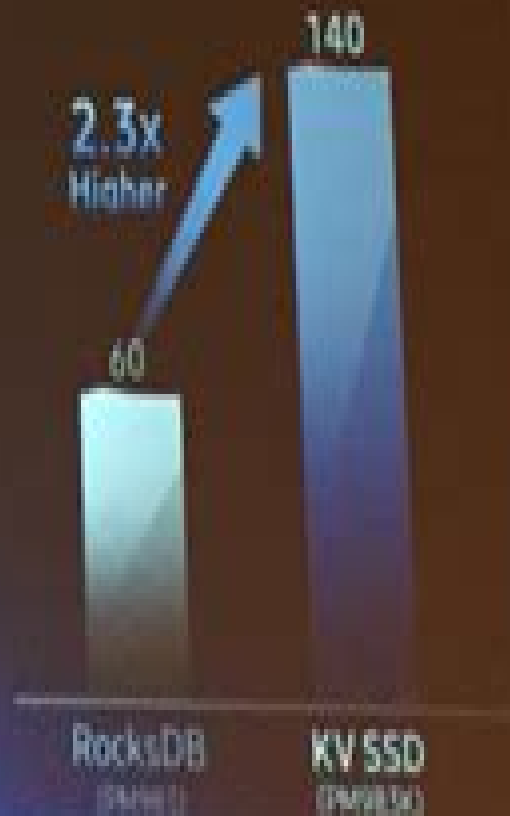
Performance Scaling



Write Amplification



Performance per SSD



Samsung Key Value Ssd Enables High Performance Scaling

Yanqin Jin



Samsung Key Value Ssd Enables High Performance Scaling:

In-/Near-Memory Computing Daichi Fujiki,Xiaowei Wang,Arun Subramaniyan,Reetuparna Das,2022-05-31 This book provides a structured introduction of the key concepts and techniques that enable in near memory computing For decades processing in memory or near memory computing has been attracting growing interest due to its potential to break the memory wall Near memory computing moves compute logic near the memory and thereby reduces data movement Recent work has also shown that certain memories can morph themselves into compute units by exploiting the physical properties of the memory cells enabling in situ computing in the memory array While in and near memory computing can circumvent overheads related to data movement it comes at the cost of restricted flexibility of data representation and computation design challenges of compute capable memories and difficulty in system and software integration Therefore wide deployment of in near memory computing cannot be accomplished without techniques that enable efficient mapping of data intensive applications to such devices without sacrificing accuracy or increasing hardware costs excessively This book describes various memory substrates amenable to in and near memory computing architectural approaches for designing efficient and reliable computing devices and opportunities for in near memory acceleration of different classes of applications

Computerworld ,2006-08-28 For more than 40 years Computerworld has been the leading source of technology news and information for IT influencers worldwide Computerworld s award winning Web site Computerworld com twice monthly publication focused conference series and custom research form the hub of the world s largest global IT media network

Designing Fast, Resilient and Heterogeneity-aware Key-value Storage on Modern HPC Clusters Dipti Shankar,2019 With the recent emergence of in memory computing for Big Data analytics memory centric and distributed key value storage has become vital to accelerating data processing workloads in high performance computing HPC and data center environments This has led to several research works focusing on advanced key value store designs with Remote Direct Memory Access RDMA and hybrid DRAM NVM storage designs However these existing designs are constrained by the blocking store retrieve semantics incurring additional complexity with the introduction of high data availability and durability requirements To cater to the performance scalability durability and resilience needs of the diverse key value store based workloads e g online transaction processing offline data analytics etc it is therefore vital to fully exploit resources on modern HPC systems Moreover to maximize server scalability and end to end performance it is necessary to focus on designing an RDMA aware communication engine that goes beyond optimizing the key value store middleware for better client side latencies Towards addressing this in this dissertation we present a holistic approach to designing high performance resilient and heterogeneity aware key value storage for HPC clusters that encompasses 1 RDMA enabled networking 2 high speed NVMs 3 emerging byte addressable persistent memory devices and 4 SIMD enabled multi core CPU compute capabilities We first introduce non blocking API extensions to the RDMA Memcached client that allows an application to separate the request

issue and completion phases This facilitates overlapping opportunities by truly leveraging the one sided characteristics of the underlying RDMA communication engine while conforming to the basic Set Get semantics Secondly we analyze the overhead of employing memory efficient resilience via Erasure Coding EC in an online fashion Based on this we extend our proposed RDMA aware key value store that supports non blocking API semantics to enable overlapping the EC encoding decoding compute phases with the scatter gather communication protocol involved in resiliently storing the distributed key value data objects This work also examines durable key value store designs for emerging persistent memory technologies While RDMA based protocols employed in existing volatile DRAM based key value stores can be directly leveraged we find that there is a need for a more integrated approach to fully exploit the fine grained durability of these new byte addressable storage devices We propose RDMP KV that employs a hybrid server reply server bypass approach to durably store individual key value pair objects on the remote persistent memory equipped servers via RDMA RDMP KV s runtime can easily adapt to existing server assisted durability and emerging appliance durability RDMA capable interconnects while ensuring server scalability and remote data consistency Finally the thesis explores SIMD accelerated CPU centric hash table designs that can enable higher server throughput We propose an end to end SIMD aware key value store design SCOR KV which introduces optimistic RDMA SIMD aware client centric request response offloading protocols SCOR KV can minimize the server side data processing overheads to achieve better scalability without compromising on the client side latencies With this as the basis we demonstrate the potential performance gains of the proposed designs with online e g YCSB and offline e g in memory and distributed burst buffer over Lustre for Hadoop I O workloads on small scale and production scale HPC clusters

Modernizing Storage Device Interface for Performance and Reliability Yanqin Jin, 2017 Modern solid state drives SSDs unnecessarily confine applications to the conventional block I O interface which under utilizes SSD s internal resources leading to suboptimal performance and unsatisfactory lifetime This thesis first presents the key addressable multi log SSD KAML an SSD with a key value interface that uses a novel multi log architecture and stores data as variable sized records rather than fixed sized sectors Exposing a key value interface allows applications to remove a layer of indirection between application level keys and data stored in the SSD KAML also provides native support for fine grained atomicity and isolation We have implemented a prototype of KAML on an SSD development platform and results show that KAML outperforms conventional systems by up to 4 0X Existing SSDs also provide flash based out of band OOB data that can only be updated on a conventional write Consequently the metadata stored in their OOB region lack flexibility due to the idiosyncrasies of flash memory incurring unnecessary flash write operations detrimental to device lifetime This thesis also presents PebbleSSD an SSD with byte addressable metadata or BAM as a mechanism exploiting the nonvolatile byte addressable random access memory NVRAM inside the SSD With BAM PebbleSSD can support a range of useful features to improve its lifetime by reducing redundant flash writes We have implemented a prototype of PebbleSSD on an SSD development platform and

experimental results demonstrate that PebbleSSD can reduce the amount of data written by log structured file systems during log cleaning by up to 99% and reduce file system level write amplification by up to 33% for a number of workloads. Finally, previous proposals for SSDs with new interfaces suffer from the limitation caused by one at a time design approach. To overcome this limitation, the thesis presents Willow, a user-programmable SSD with programmability as a central feature. Willow allows programmers to augment and extend the semantics of an SSD with application-specific features without compromising file system protections. We demonstrate the effectiveness and flexibility of Willow by implementing support for atomicity as an example. We find that defining SSD semantics in software is easy and beneficial and that Willow makes it feasible for database transaction processing workload to benefit from a customized SSD interface.

Reducing DRAM Footprint to Scale Data Store Systems Assaf Eisenman, 2019. Data-intensive applications like databases, recommender systems, and key-value caches typically consume a large amount of DRAM in order to provide high performance operations. However, DRAM is a relatively expensive storage medium that is facing major scaling challenges. Storage technologies such as Non-Volatile Memory (NVM) and flash can potentially be a lower cost alternative to DRAM but introduce several challenges due to their limited read and write bandwidth, higher latency, and limited endurance. This dissertation focuses on how to exploit the application properties to mask these challenges. It provides the design and implementation of three novel and practical data store systems that significantly reduce the DRAM footprint by utilizing various methods to overcome the device limitations. We present MyNVM, a SQL database that reduces DRAM usage by leveraging NVM as a second-level cache while providing comparable latency and queries per second (QPS) as MyRocks on a server with a much larger amount of DRAM. It introduces novel solutions to the challenges of replacing DRAM with NVM, including using small block sizes with a partitioned index, aligning blocks post-compression to reduce read bandwidth, utilizing dictionary compression, implementing an admission control policy, as well as replacing interrupts with a hybrid polling mechanism. Unfortunately, using NVM solely as a cache may not be sufficient for highly performance-sensitive applications such as real-time recommender systems. We present Bandana, a storage system for deep learning models that uses NVM as the primary storage medium. Typical large-scale recommender systems use deep learning models that are stored on a large amount of DRAM and rely on embeddings, which consume most of the required memory. The main challenge in storing embeddings on NVM is its limited read bandwidth compared to DRAM. Bandana uses two primary techniques to address this limitation: first, it stores embedding vectors that are likely to be read together in the same physical location using hypergraph partitioning, and second, it decides the number of embedding vectors to cache in DRAM by simulating dozens of small caches. These techniques allow Bandana to increase the effective read bandwidth of NVM by 2-3x and thereby significantly reduce the total cost of ownership. Even when providing sufficient performance, the adoption of NVM and flash has been limited in write-heavy use cases due to their limited durability. Key-value caches, for example, need to frequently insert, update, and evict small objects. This causes excessive writes

and erasures on flash storage which significantly shortens the lifetime of flash. We present Flashield, a hybrid key value cache that uses DRAM as a filter to control and limit writes to flash. Flashield performs lightweight machine learning admission control to predict which objects are likely to be read frequently without getting updated. These objects, which are prime candidates to be stored on flash, are written to flash in large chunks sequentially. In order to efficiently utilize the cache's available memory, Flashield utilizes a novel in-memory index for the variable-sized objects stored on flash that requires only 4 bytes per object in DRAM. Compared to state-of-the-art systems that suffer a write amplification of 2.5 or more, Flashield maintains a median write amplification of 0.5 since many filtered objects are never written to flash at all without any loss of hit rate or throughput.

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