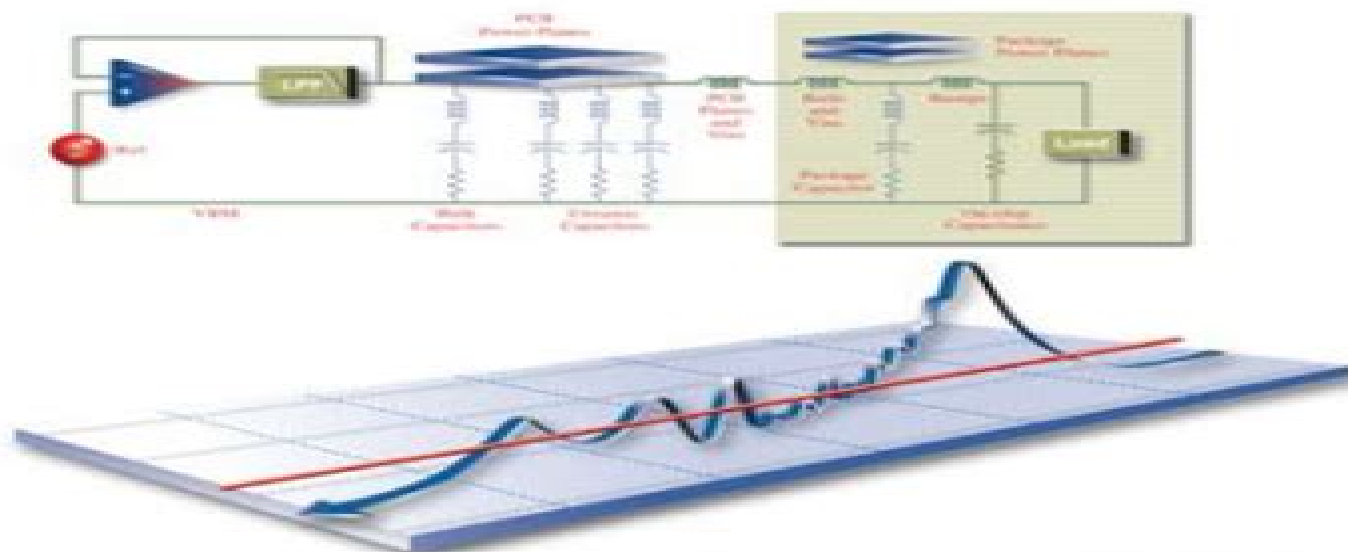


Principles of Power Integrity for PDN Design

Robust and Cost Effective Design for
High Speed Digital Products

SIMPLIFIED



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Principles of Power Integrity for PDN Design?Simplified Larry Bogatin D. Smith,2017 **Principles of Power Integrity for PDN Design--Simplified** Larry D. Smith,Eric Bogatin,2017-04-06 Consistently Design PDNs That Deliver Reliable Performance at the Right Cost Too often PDN designs work inconsistently and techniques that work in some scenarios seem to fail inexplicably in others This book explains why and presents realistic processes for getting PDN designs right in any new product Drawing on 60 years of signal and power integrity experience Larry Smith and Eric Bogatin show how to manage noise and electrical performance and complement intuition with analysis to balance cost performance risk and schedule Throughout they distill the essence of complex real world problems quantify core principles via approximation and apply them to specific examples For easy usage dozens of key concepts and observations are highlighted as tips and listed in quick chapter ending summaries Coverage includes A practical start to finish approach to consistently meeting PDN performance goals Understanding how signals interact with interconnects Identifying root causes of common problems so you can avoid them Leveraging analysis tools to efficiently explore design space and optimize tradeoffs Analyzing impedance related properties of series and parallel RLC circuits Measuring low impedance for components and entire PDN ecologies Predicting loop inductance from physical design features Reducing peak impedances from combinations of capacitors Understanding power and ground plane properties in the PDN interconnect Taming signal integrity problems when signals change return planes Reducing peak impedance created by on die capacitance and package lead inductance Controlling transient current waveform interactions with PDN features Simple spreadsheet based analysis techniques for quickly creating first pass designs This guide will be indispensable for all engineers involved in PDN design including product board and chip designers system hardware component and package engineers power supply designers SI and EMI engineers sales engineers and their managers Power Integrity for I/O Interfaces Vishram S. Pandit,Woong Hwan Ryu,Myoung Joon Choi,2010-10-13 Foreword by Joungcho Kim The Hands On Guide to Power Integrity in Advanced Applications from Three Industry Experts In this book three industry experts introduce state of the art power integrity design techniques for today s most advanced digital systems with real life system level examples They introduce a powerful approach to unifying power and signal integrity design that can identify signal impediments earlier reducing cost and improving reliability After introducing high speed single ended and differential I O interfaces the authors describe on chip package and PCB power distribution networks PDNs and signal networks carefully reviewing their interactions Next they walk through end to end PDN and signal network design in frequency domain addressing crucial parameters such as self and transfer impedance They thoroughly address modeling and characterization of on chip components of PDNs and signal networks evaluation of power to signal coupling coefficients analysis of Simultaneous Switching Output SSO noise and many other topics Coverage includes The

exponentially growing challenge of I/O power integrity in high speed digital systems PDN noise analysis and its timing impact for single ended and differential interfaces Concurrent design and co simulation techniques for evaluating all power integrity effects on signal integrity Time domain gauges for designing and optimizing components and systems Power signal integrity interaction mechanisms including power noise coupling onto signal trace and noise amplification through signal resonance Performance impact due to Inter Symbol Interference ISI crosstalk and SSO noise as well as their interactions Validation techniques including low impedance VNA measurements power noise measurements and characterization of power to signal coupling effects Power Integrity for I/O Interfaces will be an indispensable resource for everyone concerned with power integrity in cutting edge digital designs including system design and hardware engineers signal and power integrity engineers graduate students and researchers

Signal and Power Integrity, Simplified Eric Bogatin, 2010 [Power Integrity Modeling and Design for Semiconductors and Systems](#) Madhavan Swaminathan, Ege Engin, 2007-11-19 The First Comprehensive Example Rich Guide to Power Integrity Modeling Professionals such as signal integrity engineers package designers and system architects need to thoroughly understand signal and power integrity issues in order to successfully design packages and boards for high speed systems Now for the first time there s a complete guide to power integrity modeling everything you need to know from the basics through the state of the art Using realistic case studies and downloadable software examples two leading experts demonstrate today s best techniques for designing and modeling interconnects to efficiently distribute power and minimize noise The authors carefully introduce the core concepts of power distribution design systematically present and compare leading techniques for modeling noise and link these techniques to specific applications Their many examples range from the simplest using analytical equations to compute power supply noise through complex system level applications The authors Introduce power delivery network components analysis high frequency measurement and modeling requirements Thoroughly explain modeling of power ground planes including plane behavior lumped modeling distributed circuit based approaches and much more Offer in depth coverage of simultaneous switching noise including modeling for return currents using time and frequency domain analysis Introduce several leading time domain simulation methods such as macromodeling and discuss their advantages and disadvantages Present the application of the modeling methods on several advanced case studies that include high speed servers high speed differential signaling chip package analysis materials characterization embedded decoupling capacitors and electromagnetic bandgap structures This book s system level focus and practical examples will make it indispensable for every student and professional concerned with power integrity including electrical engineers system designers signal integrity engineers and materials scientists It will also be valuable to developers building software that helps to analyze high speed systems

Power Integrity for I/O Interfaces Vishram S. Pandit, Myoung Joon Choi, Woong Hwan Ryu, Woong Ryu, Myoung Choi, 2010 Foreword by Joungho Kim The Hands On Guide to Power Integrity in Advanced Applications from Three Industry

Experts In this book three industry experts introduce state of the art power integrity design techniques for today s most advanced digital systems with real life system level examples They introduce a powerful approach to unifying power and signal integrity design that can identify signal impediments earlier reducing cost and improving reliability After introducing high speed single ended and differential I O interfaces the authors describe on chip package and PCB power distribution networks PDNs and signal networks carefully reviewing their interactions Next they walk through end to end PDN and signal network design in frequency domain addressing crucial parameters such as self and transfer impedance They thoroughly address modeling and characterization of on chip components of PDNs and signal networks evaluation of power to signal coupling coefficients analysis of Simultaneous Switching Output SSO noise and many other topics Coverage includes The exponentially growing challenge of I O power integrity in high speed digital systems PDN noise analysis and its timing impact for single ended and differential interfaces Concurrent design and co simulation techniques for evaluating all power integrity effects on signal integrity Time domain gauges for designing and optimizing components and systems Power signal integrity interaction mechanisms including power noise coupling onto signal trace and noise amplification through signal resonance Performance impact due to Inter Symbol Interference ISI crosstalk and SSO noise as well as their interactions Validation techniques including low impedance VNA measurements power noise measurements and characterization of power to signal coupling effects Power Integrity for I O Interfaces will be an indispensable resource for everyone concerned with power integrity in cutting edge digital designs including system design and hardware engineers signal and power integrity engineers graduate students and researchers

Power Integrity for I/O Interfaces Vishram S. Pandit,1900 Foreword by Joungho Kim The Hands On Guide to Power Integrity in Advanced Applications from Three Industry Experts In this book three industry experts introduce state of the art power integrity design techniques for today s most advanced digital systems with real life system level examples They introduce a powerful approach to unifying power and signal integrity design that can identify signal impediments earlier reducing cost and improving reliability After introducing high speed single ended and differential I O interfaces the authors describe on chip package and PCB p

Power Integrity Modeling and Design for Semiconductors and Systems Madhavan Swaminathan,A. Ege Engin,2007 The First Comprehensive Example Rich Guide to Power Integrity Modeling Professionals such as signal integrity engineers package designers and system architects need to thoroughly understand signal and power integrity issues in order to successfully design packages and boards for high speed systems Now for the first time there s a complete guide to power integrity modeling everything you need to know from the basics through the state of the art Using realistic case studies and downloadable software examples two leading experts demonstrate today s best techniques for designing and modeling interconnects to efficiently distribute power and minimize noise The authors carefully introduce the core concepts of power distribution design systematically present and compare leading techniques for modeling noise and link these techniques to specific applications Their many examples range from the

simplest using analytical equations to compute power supply noise through complex system level applications The authors Introduce power delivery network components analysis high frequency measurement and modeling requirements Thoroughly explain modeling of power ground planes including plane behavior lumped modeling distributed circuit based approaches and much more Offer in depth coverage of simultaneous switching noise including modeling for return currents using time and frequency domain analysis Introduce several leading time domain simulation methods such as macromodeling and discuss their advantages and disadvantages Present the application of the modeling methods on several advanced case studies that include high speed servers high speed differential signaling chip package analysis materials characterization embedded decoupling capacitors and electromagnetic bandgap structures This book s system level focus and practical examples will make it indispensable for every student and professional concerned with power integrity including electrical engineers system designers signal integrity engineers and materials scientists It will also be valuable to developers building software that helps to analyze high speed systems

Power Integrity Analysis and Management for Integrated Circuits (paperback) Raj Nair,Donald Bennett,2010-05-07 New Techniques and Tools for Ensuring On Chip Power Integrity Down to Nanoscale As chips continue to scale power integrity issues are introducing unexpected project complexity and cost In this book two leading industry innovators thoroughly discuss the power integrity challenges that engineers face in designing at nanoscale levels introduce new analysis and management techniques for addressing these issues and provide breakthrough tools for hands on problem solving Raj Nair and Dr Donald Bennett first provide a complete foundational understanding of power integrity including ULSI issues practical aspects of power delivery and the benefits of a total power integrity approach to optimizing chip physical designs They introduce advanced power distribution network modeling design and analysis techniques that highlight abstraction and physics based analysis while also incorporating traditional circuit and field solver based approaches They also present advanced techniques for floorplanning and power integrity management and help designers anticipate emerging challenges associated with increased integration Anasim RLCSim exe a new tool for power integrity aware floorplanning is downloadable for free at anasim.com category software The authors Systematically explore power integrity implications analysis and management for integrated circuits Present practical examples and industry best practices for a broad spectrum of chip design applications Discuss distributed and high bandwidth voltage regulation differential power path design and the significance of on chip inductance to power integrity Review both traditional and advanced modeling techniques for integrated circuit power integrity analysis and introduce continuum modeling Explore chip package and board interactions for power integrity and EMI and bring together industry best practices and examples Introduce advanced concepts for power integrity management including non linear capacitance devices impedance modulation and active noise regulation Power Integrity Analysis and Management for Integrated Circuits coverage of both fundamentals and advanced techniques will make this book indispensable to all engineers responsible for signal integrity

power integrity hardware or system design especially those working at the nanoscale level [Power Integrity Analysis and Management for Integrated Circuits](#) Rajendran Nair,2010 **Power Distribution Network Design Methodologies** Istvan Novák,2008 A series of cogently written articles by 49 industry experts this collection fills the void on Power Distribution Network PDN design procedures and addresses such related topics as DC DC converters selection of bypass capacitors DDR2 memory systems powering of FPGAs and synthesis of impedance profiles Through these contributions from such leading companies as Sun Microsystems Sanyo IBM Hewlett Packard Intel and Rambus readers will come to understand why books on power integrity are only now becoming available to the public and can relate these topics to current industry trends

Power Distribution Network Design Methodologies István Novák,2021-08-17 The Faraday Press Edition of Istvan Novák's historic Power Distribution Network Design Methodologies brings to print important coverage of power system design topics including circuit board layout strategies capacitor characterization and selection controlled impedance design and guidance for system level engineering Power Distribution Network PDN design procedures are covered in practical detail covering topics including the buck converter topology the proper selection and placement of bypass capacitors power requirements of memory systems powering FPGAs and designing controlling wideband power delivery impedances As clock speeds and power density requirements progress the challenges of a robust system design becomes more and more important Power Distribution Network Design is a valuable resource for the global community of power supply designers

[The Printed Circuit Designer's Guide To... Power Integrity by Example](#) Fadi Deek,2017-11-30 There are many factors to consider when aiming to establish and maintain power integrity from cavity thickness to the presence or absence of a voltage regulator Written by signal power integrity specialist Fadi Deek of Mentor A Siemens Business this micro eBook provides a thorough investigation of power distribution network performance Deek addresses problematic issues within electronic transmissions and presents a variety of simulations and analyses in every chapter After you've read this eBook you will better understand cause effect relationships between varying factors and how to consider these when making design decisions

[Power Integrity for Nanoscale Integrated Systems](#) Raj Nair,Masanori Hashimoto,2014-03-19 Publisher's Note Products purchased from Third Party sellers are not guaranteed by the publisher for quality authenticity or access to any online entitlements included with the product Proven methods for noise tolerant nanoscale integrated circuit design This leading edge guide discusses the impact of power integrity from a design perspective emphasizing phenomena and problems induced by power integrity degradation and the latest design trends including low power design Power Integrity for Nanoscale Integrated Systems describes how these problems can be forecast early in the design process and the countermeasures that can be used to address them such as the inclusion of inductance and accurate modeling for PI analysis as well as robust circuit design Detailed examples and a case study on the IBM POWER7 processor illustrate real world applications of the techniques presented in this practical resource Coverage includes Significance of power integrity for integrated circuits

Supply and substrate noise impact on circuits Clock generation and distribution with power integrity Signal and power integrity design for I/O circuits Power integrity degradation and modeling Lumped distributed and 3D modeling for power integrity Chip temperature and PI impact Low power techniques and PI impact Power integrity case study using the IBM POWER7 processor chip Carbon nanotube interconnects for power delivery *Power Integrity* Steven M. Sandler, 2014-07-29 PROVEN TECHNIQUES FOR GENERATING HIGH FIDELITY MEASUREMENTS Power Integrity Measuring Optimizing and Troubleshooting Power Related Parameters in Electronics Systems provides field tested techniques for producing high fidelity measurements using the appropriate equipment The book thoroughly discusses measurement guidelines test instrument selection and use connecting the equipment to the device being tested and interpreting the acquired data The latest electronics technologies and their impact on measurement are discussed Detailed photographs screenshots schematics and equations are included throughout this practical guide Learn how to accurately measure Impedance Stability Power supply rejection ratio PSRR Reverse transfer and crosstalk Step load response Ripple and noise Edges High frequency impedance *Power Distribution Network Design Methodologies* Dr. Istvan Novak, 2008-06

Signal and Power Integrity-simplified (Third Edition) Eric Bogatin, 2021 *System Level Design of Power Distribution Network for Mobile Computing Platforms* Amirali Shayan Arani, 2011 Providing a reliable power distribution network PDN is a critical design challenge for mobile system on chip platforms A well designed power distribution network should be robust enough to support chipset performance while avoids eroding product profit margins through excessive design guardbanding The solution space between these two requirements is small for PDN designs On one hand an inadequate PDN design can lead to test failures missed performance targets and intermittent functional problems in the field On the other hand some of the more direct PDN improvements such as adding on die regulators on package discrete decoupling capacitors and package layers increase die and package size and could cost tens to hundreds of millions of dollars per product line Mobile platform PDN design is challenging due to limited form factor heterogeneous congested blocks with different design specifications and adoption of multiple low power techniques and modes Therefore it is important to develop a set of PDN design methodologies and analysis tools that can guide the product development from product inception through test and debug This dissertation focuses on different aspects of reliable power distribution network design for mobile computing platforms First we propose an early stage power distribution modeling framework to analyze the power distribution during design cycle We consider the complete closed loop system from voltage regulation module printed circuit board package and silicon die for the co simulation Subsequently an enhanced time domain and frequency domain analysis flow is proposed For assessing the performance of the power distribution in the presence of multiple functional power modes we introduce a worst case current loading generation The current generation algorithm synthesizes the functional vector load based on anti resonance i.e resonance aware and rogue wave to gain more realistic worst case voltage variation We investigate the impact of power

distribution variation on the performance of mobile processors We estimate the impact of power integrity considerations on low power processor performance through pre silicon simulation and post silicon measurements We present a predictive performance model under voltage and temperature variations to guide the designers in the early stages of design As part of this effort new emerging technologies for design of power distribution are investigated A reliability aware model for 3D stacked chips is developed The model considers the complete system including Through Silicon Via TSV substrate noise and stacked dies from both time and frequency domain perspectives Finally we discuss the recent efficient direction towards on die regulations for design and optimization of the Linear Dropout based PDN under worst performance In summary the complete framework of this thesis aims to provide the means for designing robust power distribution for current evolving mobile computing platforms

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