

Active Matrix Driving and Circuit Simulation

Makoto Watanabe

*Sony Mobile Display Corporation
Japan*

1. Introduction

This chapter explains the principle of active matrix driving which is the most popular driving method used in current liquid crystal displays (LCDs). It then discusses issues that designers must overcome to avoid the malfunctioning and introduces a liquid crystal model for conducting circuit simulations to optimize the circuit parameters efficiently.

1.1 Equivalent circuit of a pixel in LCDs

The equivalent circuit of a pixel operated by active matrix driving is shown in Fig. 1.

Data lines are connected to a data driver for generating the signal pulses for the picture data. Scan lines are connected to a scan driver for generating the scan pulses which enable the addressing driving. V_{sig} and V_g are applied to the data lines and scan lines, respectively. The thin film transistor (TFT) has three terminals of MOS transistors, and each terminal gate, drain, and source is connected to a scan line, a data line, and a pixel electrode, respectively. C_{gs} means the parasitic capacitance between the gate and source terminal in the TFT. Liquid crystal is injected into the gap between the pixel electrode and the counter backplane electrode, and it forms a liquid crystal cell capacitance (C_{lc}). C_{lc} is a variable capacitor that changes value according to the applied voltage between the pixel electrode and a counter backplane electrode. The voltage of the pixel electrode and counter backplane electrode are denoted by V_{pix} and V_{com} , respectively. The storage capacitor is denoted C_{sc} , and it is connected in parallel to C_{lc} . Its function is to hold charges on a pixel electrode while the TFT is switched off.

1.2 Timing chart for each signal pulse

Fig. 2 shows the wave forms applied to each bus line and electrode. The period during which the pixel electrode voltage (V_{pix}) is higher than the counter electrode voltage (V_{com}) is called the "plus frame" (Fig.2 (a)), whereas the period during which V_{pix} is lower than V_{com} is called the "minus frame" (Fig.2 (b)). The plus and minus frames are switched every frame period (T_f).

When the voltage of the gate terminal connecting to the scan line rise to a high level, the resistance between the drain and source terminals becomes very low (R_{on}). As a result, electrical charges flow into the pixel electrode from the data line till the voltage of the pixel electrode achieves the voltage of the data line during the writing time (T_w). This process is called the "Charge Process". When the voltage of the scan line starts to drop, the pixel electrode voltage shows a negative shift ΔV_{fd} because of the coupling with the gate terminal

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Abstract This dissertation presents two circuit simulation techniques to accelerate the simulation time for time domain transient circuit simulation and circuit thermal analysis. Matrix exponential method is one of the state of the art methods for millionth order time domain circuit simulations due to its explicit nature and global stability. The matrix exponential is commonly computed by Krylov subspace methods which become inefficient when the circuit is stiff, namely when the time constants of the circuit differ by several orders. The truncated Faber series is suitable for accurate evaluation of the matrix exponential even under a highly stiff system matrix arising from practical circuits. Experiments have shown that the proposed approach is globally stable, highly accurate, and parallelizable and avoids excessive memory storage demanded by Krylov subspace methods. Another major issue in circuit simulation is thermal circuit analysis. The use of Hierarchical matrix (H matrix) in the efficient finite element based (FE) based direct solver implementation for both steady and transient thermal analyses of three dimensional integrated circuits (3D ICs) is proposed. H matrix was shown to provide a data sparse way to approximate the matrices and their inverses with almost linear space and time complexities. This is also true for FE based transient analysis of thermal parabolic partial differential equations (PDEs). Specifically, the stiffness matrix from a FE based steady and transient thermal analysis can be represented by H matrix without approximation and its inverse and Cholesky factors can be evaluated by H matrix with controlled accuracy. This thesis shows that the memory and time complexities of the solver are bounded by $O(k_1 N \log N)$ and $O(K_1 \text{DEGREES}^2 N \log \log \text{DEGREES}^2 N)$ respectively for very large scale thermal systems where k_1 is a small quantity determined by accuracy requirements and N is the number of

unknowns in the system Numerical results validate and demonstrate the effectiveness of the proposed method in terms of predicted theoretical scalability DOI 10 5353 th_b5090009 Subjects Integrated circuits Data processing

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