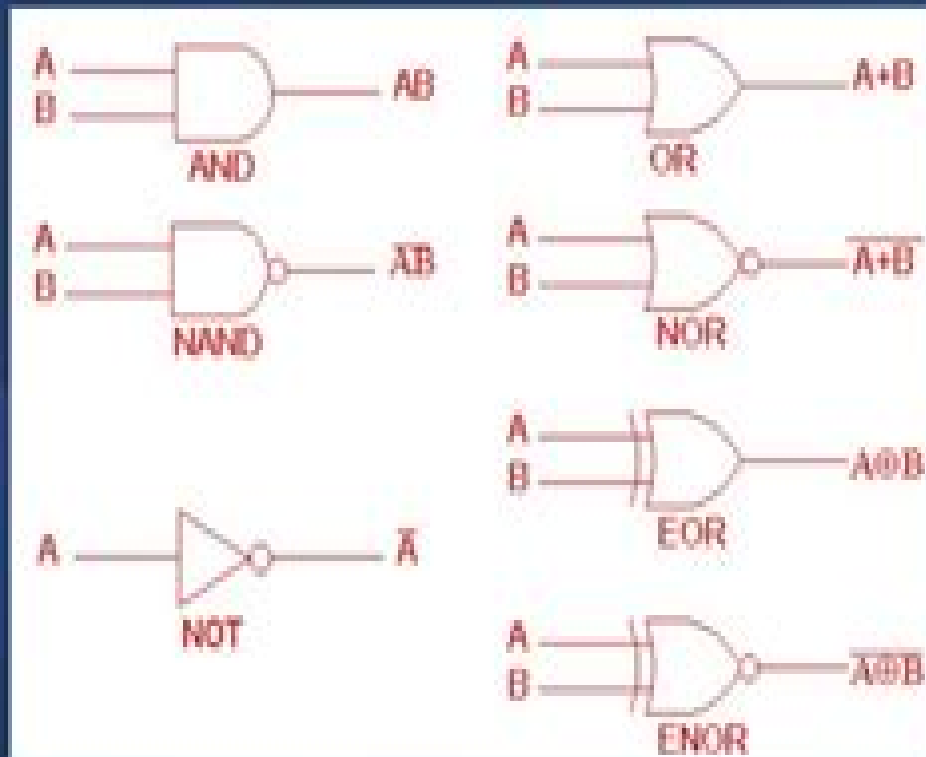


System Verilog Tutorial

Combinational Logic Design



```
// Code your design here
timescale 1ns/1ns
module gates(a, b, and, andn, nor, or, eor, norx, xorx);
    input logic a, b;
    output reg and, andn, nor, or, eor, norx, xorx;

    always @(a or b)
    begin
        assign and = (a & b);
        $display("and logical operator");

        assign andn = ~(a & b);
        $display("and logical operator");

        assign or = (a | b);
        $display("or logical operator");

        assign nor = ~(a | b);
        $display("nor logical operator");

        assign eor = ((a & ~b) | (~a & b));
        $display("eor logical operator");

        assign xorx = ((a & ~b) | (~a & b));
        $display("xor logical operator");
    end
endmodule
```

Combinational Logic Design With Verilog

AN Whitehead



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